CMOS device architecture evolution and its impact on surface preparation and cleaning for N2 and beyond

Naoto Horiguchi

Imec, Leuven, Belgium
CMOS device scaling challenges

Device architecture evolution and its impact on surface preparation and cleaning
- Nanosheet
- Forksheet
- Complementary FET (CFET)
- Buried power rail

Summary
Current Scaling Challenges for Sub-6T cells

6T With Standard Power Rail

Key Challenges
• Gate & Fin pitch scaling has slowed down ➔ Compensated by track height scaling (= Fin # reduction)
• Scaling of NP spacing
• Need for wide power rails to minimize IR drop
5T cells in the future

5T With Buried Power Rail (BPR)

What’s new
• Single fin architecture with stacked nanosheet channel
• Scaling of NP spacing by Forksheet or CFET (not shown).
• High aspect ratio buried power rails in STI/substrate
Device Architecture Roadmap

Single Device

FinFET

Nanosheet

Forksheat

CMOS device architecture

CFET

PFET

NFET

1st introduction of GAA

Evolution from 2D Nanosheet

Revolutionary 3D

Revolutionary 3D
FINFET SCALING CHALLENGES

Fins are getting taller, thinner, and closer.

7.5T 2 fins  6T 2 fins  5T 1 fin

Fin de-population is required for standard cell scaling.

Drive strength ➔ Variability ➔
EVOLUTION FROM FINFET TO NANOSHEET

Nanosheet Advantages

- Maximized effective width → Drive current increase
- Improved short-channel control due to gate-all-around
- Variable device width for design flexibility
Nano Sheet process flow

- Starting material: Bulk Si wafer
- Ground plane I/I + anneal
- SiGe/Si/SiGe/Si epitaxy (a)
- Spacer-defined fin patterning (SADP)
- Low-temperature STI filling
- Dummy gate patterning
- RT extension I/I + Spacer formation
- Inner spacer + Embedded SD epi (b)
- ILD0 deposition/CMP
- Dummy poly/oxide removal
- Si channel release by SiGe etch (c)
- Gate dielectric (IL-SiO₂/HfO₂) dep.
- Work function (WF) metal deposition & patterning
- Fill metal (W) deposition/CMP
- Contact formation + M1 BEOL

Nanosheet flow is similar as FinFETs except for Si/SiGe stack fins, inner spacer, nanosheet channel release and WFM patterning.
Nanosheet integration needs SiGe & dielectric isotropic selective etches.
• High etch selectivity and post etch surface clean are key.
N-P SPACE SCALING BY FORKSHEET AND CFET

**Forksheet Advantages**

- N-P space can be defined by dielectric wall

**CFET (Complementary FET) Advantages**

- N-P space becomes vertical space due to stacked NMOS & PMOS
Nanosheet vs Forksheet

Nanosheet + Dielectric wall = Forksheet
Work Function Metal Patterning: Nanosheet vs Forksheet

Nanosheet RMG process flow

SOC HM patterning

High AR HM patt. necessary.

WFM etch

Lateral over etch margin increase N/P space.

WFM Overetch

Forksheet RMG process flow

PMOS Nanosheet channel

Dielectric wall

NMOS Nanosheet channel

Low AR HM patt.

Dielectric wall stops WFM over etch

WFM etch/Over etch

Smaller N-P space is enabled by dielectric wall in forksheet.
Forksheet process flow uses backbone of nanosheet

Dielectric wall formation and its impact in subsequent processes

- Nanosheet stack patterning/STI CMP (BPR etch + metallization) optional
- Nanosheet stack reveal
- **FSH dielectric wall formation**
- Gate patterning
- Spacer and fin recess
- **Inner spacer**
- Source/drain epitaxy
- ILD0 CMP
- **RMG**
- Gate recess + cut
- Gate plug
- M0A patterning + metallization
- MINT/VINT (dual damascene)

**Forksheet process flow is similar as nanosheet flow.**

- Dielectric wall formation and its impact on subsequent module are important.

P. Weckx et al IEDM 2019
Dielectric wall integration

Dielectric wall formation process flow

Nanosheet reveal

Wall dielectric deposition

Wall isotropic etch

Dummy oxide deposition

8-16nm

80nm

Inner spacer & CMOS SD epi HM patterning

WFM HM patterning

Forksheet key process steps
• Dielectric wall isotropic etch
• HM patterning for CMOS epi & WFM to avoid dielectric wall loss

+ Nanosheet critical steps
• Si/SiGe STI, inner spacer, channel release, WFM patterning
Complementary FET (CFET)

- CMOS-like to single device-like foot-print
- N-P space in vertical direction has no area penalty.

Demonstration of Monolithic CFET

S. Subramanian et al VLSI2020
CFET integration options

Monolithic CFET
- STI w/ SiGe sac. layer
- Bottom SD & contact
- Top SD & contact
- RMG

Sequential CFET
- Bottom device process
- Wafer bonding
- Top device process
- Top ch. Layer transfer
- Bottom ch.

CFET integration options
• Monolithic: Bulk device integration from bottom to top
• Sequential: Bottom device process $\rightarrow$ Wafer bonding $\rightarrow$ Top device process
Monolithic CFET Flow

Cost effective but need high ar patterning & complex vertical integ.

Challenges:
- Cleaning in high aspect ratio trench
- Vertical edge placement control by precise CMP and etch back (see next slide)

S. Subramanian et al VLSI2020
In monolithic CFET integration, vertical edge placement controlled by CMP and etch back. Precise CMP and etch back control is necessary.
Sequential CFET flow

Challenge: Defect-free wafer bonding w/ scaled bonding oxide thickness (~30nm)
(Bonding oxide CMP uniformity & post CMP clean)
Wafer bonding defect control

Underlying topography induces bonding voids, especially at thin bonding oxide.

- Topography control by CMP is important
Buried Power Rails (BPR)

- BPR free up space in BEOL. → Area scaling.
- BPR line aspect ratio can be increased. → IR drop improvement
BPR and VBPR process flow

**BPR process flow**

- STI Fill & CMP
- BPR etch & Dielectric barrier
- BPR metallization, CMP
- BPR metal recess
- Plug fill & CMP
- Oxide recess

**BPR metal clean to avoid metal contamination in FEOL**

**M0A/VBPR process flow**

- RMG/Gate plug
- M0A etch
- M0A/VBPR fill & CMP
- VBPR litho
- VBPR etch
- Post VBPR etch clean on SD and BPR
# BPR/VBPR metal candidates

<table>
<thead>
<tr>
<th>BPR metal</th>
<th>W</th>
<th>Ru</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEOL process compatibility</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal recess</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electromigration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Line Resistance</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VBPR metal</th>
<th>Co</th>
<th>Mo</th>
<th>Ru</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compatibility w/ M0A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal recess</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electromigration</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Via Resistance</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- W and Co are first candidates for BPR and VBPR.
- Ru and Mo have potential to improve line and via resistance ➔ Need proper CMP/clean

A. Gupta et al VLSI 2020

Q. T. Le et al SPCC 2020
Summary

- **CMOS device scaling challenges**
  - Track height (# of metal lines/standard cell) scaling to compensate pitch scaling slow down
    - Fin #/device reduction
    - N-P space reduction
    - Power line width scaling

- **Device architecture evolution and its impact on surface preparation and clean**
  - Nanosheet: Enables **single fin architecture** by wider device width/footprint than FinFET
    - SiGe & dielectric **high selective isotropic etch** is necessary for inner spacer & channel release. **Post-etch clean surface** is important for SD epi and gate stack.
  - Forksheet: Dielectric wall reduces **N-P space** than nanosheet.
    - **Dielectric wall isotropic selective etch** is additional step for FS. Dielectric wall loss has to be minimized in subsequent modules, such as SD epi and RMG.
  - CFET: **Smaller device CMOS footprint** than NS & FS, **N-P space is vertical** direction
    - Monolithic: **Post etch clean in high AR trench. Vertical edge placement control** by precise CMP & etch back.
    - Sequential: **Defect-free wafer bonding** with **thin bonding oxide** by **good CMP control** and **clean**
  - Buried Power Rail: **Power line area reduction** by high aspect ratio line buried in STI/substrate
    - **Proper clean** is necessary to integrate **BPR metal w/o contamination issues.**
    - **CMP/clean** for **new low resistive/barrier-less metal**, such as Mo and Ru, needs to be developed for the future.